In the Specification:

Please replace the paragraph beginning on page 13, line 5 with the following amended paragraph:

In Fig. 3, Ton and Toff respectively denote the rising time and falling time of the gate scan signal G. The blanking period Tbk is sufficiently ~~loner~~ longer than the block control period Tb, and satisfies a condition Tbk > Tb + Ton + Toff.

Please replace the paragraph beginning on page 15, line 15 with the following amended paragraph:

The line-sequential driver IC chip 512 includes the aforementioned first through fifth parts. Also, the driver IC chip 512 has an input port having a function of selecting a six-bit input or an eight-bit input, and an output port having 384 output terminals with buffer amplifier buffers. Hence, the device 512 has a ~~capability of a~~ capability of handling a block width of 384 bits at a maximum. Further, the device 512 is designed to have, in operation, a maximum output resistance equal to or less than about 5 kΩ in order to make it possible to drive a display block having a wide data width, namely, long common signal lines. Hence, the device 512 can improve the time constant Ts of the signal lines 522 arranged in the display part 518.

Please replace the paragraph beginning on page 23, line 31 with the following amended paragraph:

The driver IC chip 220 is mounted on the TAB-IC device 206, but may be mounted in the COG (Chip On Glass) mount formation or TCP so that the chip 220 is directly mounted on the common substrate 202. In order to ~~simply~~ simplify the terminal crimping step, the TAB-IC device 206 has through lines other than the common signal lines such as clock signal lines and control lines on the data and gate sides of the TAB-IC device 206, the above through lines being connected to the printed-circuit board 200. Hence, it is not necessary to provide any component such as a flexible printed-circuit board to the liquid crystal display device 540 in order to separately provide lines corresponding to the above through lines.

Please replace the paragraph beginning on page 26, line 22 with the following amended paragraph:

As shown in Fig. 16, the liquid crystal display device 340 includes a line-sequential driver IC device 312, the analog switches 314, the gate drivers 316 and 317, the display part 318, common electrodes 336 and 338, ~~and an~~ and a static electricity prevention part 342.

Please replace the paragraph beginning on page 43, line 28 with the following amended paragraph:

As shown in Fig. 38, when the initial potential VSL0 is equal to V1, it takes a time Tr1 the pixel potential to rise up to the potential Vs. When the initial potential VSL0 is equal to V2, it takes a time Tr2 for the pixel potential to reach the potential Vs. When the initial potential VSL0 is equal to V3, it takes a time Tr3 for the pixel potential to reach the potential Vs. The potentials V1, V2 and V3 have a relationship such that V1 > V2 > V3, while the rising times Tr1, Tr2 and Tr3 have a relationship such that Tr1 < Tr2 < Tr3. As described above, the time Tr necessary for the pixel potential to reach the potential Vs depends on the initial potential VSL0 of the signal line part 612.

Please replace the paragraph beginning on page 47, line 24 with the following amended paragraph:

The reset circuit shown in Fig. 41 has a simple structure, and the reset circuit shown in Fig. 42 has a high driving ability and reduces the reset time. The n-channel MOS transistor shown in ~~fig. 45~~ Fig. 41 may be replaced by a p-channel MOS transistor. The transistor used in the configuration shown in Fig. 41 has dual gates. Similarly, the CMOS circuit may have dual gates. When the dual-gate transistors are used, the leakage currents flowing in the pixel TFTs 616 can be reduced for the signal hold period.